Digital Semiconductor StrongARM SA-110 Power Dissipation and Thermal Characteristics:

An Application Note

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This application note provides information related to the power dissipation of the SA-110 chip. It includes information on power supply sizing and ambient temperature limits, which are important to system designers. While we attempted to use reasonable values in our calculations of chip power in typical systems, system designers should repeat these calculations using values appropriate to their particular system.

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1 Introduction

This application note provides information related to the power dissipation of the SA-110 chip. It includes information about:

- Power supply sizing
- Ambient temperature limits
- Power running the loop in Dhrystone 2.1
- Power for typical applications

The power equation depends on characteristics of the system in which the SA-110 resides. While we have attempted to use reasonable values for system-dependent parameters in our calculations of chip power, system designers should repeat these calculations using values appropriate to their particular system.

2 Power Budget Philosophy

Before presenting the expressions for power consumption, it is useful to discuss power budget philosophy. To design a low-power, low-cost, high-performance microprocessor, we made several trade-offs that might limit the options available to system designers.

First, to run the internal circuitry at 160 MHz, we dedicated most of the power to the core logic. I/O power is kept low by limiting the cap on the pins and by including large caches to minimize pin activity. While the actual partition of power between the internal and external supplies varies, it is not uncommon to have 90% of the power consumed by the core of the chip for programs that exhibit reasonable cache performance.

Next, to minimize size and cost, we packaged the chip in a thin quad flat pack (TQFP) package. This package has a high thermal resistance (theta JA) that limits the power dissipation permitted, even in systems not running from batteries.

Finally, in keeping with the low-power orientation, it is assumed that the pins are driving capacitive loads. If pins are required to source or sink dc current, the system designers must consider the thermal and power supply implications in addition to the absolute maximum limit of 2 mA/pin.

3 Power Supply Sizing

The goal here is to specify the absolute maximum amount of power your system should operate at under any conditions. To accomplish this, use the following equations:

Max **Iddi** (mA) = 1.43 * max **Vddi**(V) * CPU freq(MHz)

Max **Iddx** (mA) = [7.0e-3 * max **Vddx**(V) * bus freq(MHz) * pin load(pF)]
+ [74 * max dc pin current(mA)]

The variables used in these equations are as follows:

- **Iddi**: the internal current
- Max **Vddi**: the maximum value of the internal power supply voltage in volts
- CPU freq: the internal operating frequency (that is, the PLL frequency) in MHz
- **Iddx**: the external current
- Max **Vddx:** the maximum value of the external power supply voltage in volts
- Bus freq: the bus frequency (**MCLK**) in MHz
- Pin load: the capacitance in pF on the pins driven by the SA-110
- Max dc pin current: the maximum current, mA, per output that the SA-110 is required to sink or source

The ac nature of the power consumption makes it data-dependent, thus, difficult to estimate. Table 1 contains margin beyond what is observed in Dhrystone 2.1.

Table 1 SA-110 Absolute Maximum Power

Max Vddi (V)	CPU Freq (MHz)	Max Vddx (V)	Bus Freq (MHz)	Pin Load per Pin (pF)	dc Current per Pin (mA)	Iddi (mA)	Iddx (mA)
1.8	99.4	3.6	33	20	0	256	17
1.8	161.9	3.6	33	20	0	417	17
2.2	202.4	3.6	33	20	0	637	17
2.2	202.4	3.6	66	20	0	637	33
2.1	236.2	3.6	66	20	0	709	33
2.2	202.4	3.6	66	50	0	637	83
2.2	202.4	3.6	66	20	2	637	181

4 Thermal Limits on Power Consumption

The SA-110 is designed to operate at a maximum junction temperature of 100 degrees Celsius (100°C). Because the SA-110 may be used at several power supply voltages and operating frequencies, it is necessary to consider the following:

- Power dissipation of the chip
- Thermal characteristics of the package
- System environment to translate this junction temperature to an ambient temperature specification

In typical applications, the maximum ambient temperature is limited to 70°C. In certain applications, it may be necessary to restrict the ambient temperature to a value lower than 70°C to ensure that the junction temperature does not rise above 100°C. However, the chip should never be operated at an ambient temperature greater than 70°C, even if the expressions below indicate that the junction temperature would stay below 100°C.

The procedure to determine the maximum ambient temperature is as follows:

1. Determine the maximum power dissipation for the SA-110 for the power supply voltage and operating frequency of interest using the equation given in Section 4.1.
2. Determine the junction to ambient thermal resistance (theta JA) that corresponds most closely to your system (see Section 4.2).
3. Calculate the maximum ambient temperature for which the junction temperature is below 100°C. The maximum ambient temperature is the minimum of this value and 70°C (see Section 4.3).

4.1 Maximum Power for Thermal Calculations

The maximum power of the SA-110 for use in thermal calculations is as follows:

$$\begin{aligned}\text{Power(mW)} = {} & [0.87 * \{\max \mathbf{Vddi}(V)\}^2 * \{\text{CPU freq(MHz)}\}] \\ & + [5.84\text{e-}3 * \{\max \mathbf{Vddx}(V)\}^2 * \{\text{bus freq(MHz)}\} * \{\text{pin load(pF)}\}] \\ & + [14.8 * \max \text{dc pin current(mA)} * \max \mathbf{Vddx}(v)]\end{aligned}$$

4.2 Thermal Characteristics

The device is packaged in a 144-pin TQFP plastic package. Thermal performance of the device has been characterized in several different environmental conditions. The device’s thermal performance depends on the board construction, board design, and surrounding environmental condition.

Theta JA (junction to ambient) thermal resistance of this device in a highly integrated system requiring four to six copper layer board construction is in a range of 30°C/watt to 40°C/watt. The thermal resistance in a close proximity condition (where air movement is constrained) is about 40°C/watt and in an open environment (where air circulates freely) is about 30°C/watt.

4.3 Ambient Temperature

The maximum ambient temperature is:

Max Ta = Minimum of [70°C, Calculated Max Ta]

where:

Calculated Max Ta = 100°C - [Power(mW) * 0.001 * theta JA(°C/W)]

The maximum ambient temperature for several interesting cases is shown in Table 2. For most of the cases shown, an ambient temperature of 70°C is acceptable for an open environment. For some of the higher speed cases, the ambient temperature would have to be reduced below 70°C if the chip is operated in close proximity conditions such as a personal digital assistant (PDA).

Caution: Higher CPU speeds, bus speeds, and pin loads increase the power, and some combination of these factors might require ambient temperatures below 70°C, even for the open environment case. Also, the actual maximum ambient temperature is the minimum of 70°C and the calculated maximum ambient temperature. The chip should never be operated at an ambient temperature higher than 70°C.

Table 2 Calculated Max Ta for Theta JA

Max Vddi (V)	CPU Freq (MHz)	Max Vddx (V)	Bus Freq (MHz)	Pin Load per Pin (pF)	dc Current per pin (mA)	Total Power (mW)	Calculated Max Ta in °C for Theta JA = 40°C/W	30°C/W
1.8	99.4	3.6	33	20	0	330	87	90
1.8	161.9	3.6	33	20	0	510	80	85
2.2	202.4	3.6	33	20	0	900	64	73
2.2	202.4	3.6	66	20	0	950	62	71
2.1	236.2	3.6	66	20	0	1010	60	70
2.2	202.4	3.6	66	50	0	1100	56	67
2.2	202.4	3.6	66	20	2	1060	58	68

5 Internal Power Estimates

The basis of the estimates for internal power in the SA-110 is power measurements of the chip executing the internal loop of Dhrystone 2.1. This program fits entirely in the onchip caches so that after the first pass through the loop, pin activity is limited to two writes on each pass through the loop.

Because cache misses cause the internal CPU clocks to operate at the lower bus frequency during the fill, cache misses reduce the chip power in most cases. Therefore, the power running Dhrystone 2.1 is higher than is seen in typical applications. However, because the power on CMOS chips is pattern-dependent, specification of the SA-110 power running Dhrystone 2.1 provides a well-defined point for reference. Additionally, it can be scaled in a simple manner to provide estimates for typical applications. The scaling procedure is discussed in Section 5.2.

Because the dc current on the SA-110 is low and I/O activity is limited in Dhrystone 2.1, the Dhrystone power depends only on **Vddi** and the CPU frequency:

Dhrystone 2.1 power = 404 mW * (**Vddi**(v)/1.65)^2 * (CPU freq(MHz)/161.9)

At low frequencies, the low internal dc power of the SA-110 may become significant. This effect is described in Section 5.3.

5.1 I/O Power

You can estimate bus power based on assumptions about capacitance and switching activity. In general, the dominant capacitance being switched is the capacitance of the pin node itself (including trace and loads). For I/O pins, the SA-110 contributes 12 pF to this cap.

For particularly lightly loaded pins, the capacitance of the pin pre-driver may be of interest because it switches whenever the pin switches. This cap is 2.2 pF for the MCLK and nMCLK pins and 1.1 pF for all other outputs and I/O pins.

It is difficult, if not impossible, to provide an estimate of bus switching characteristics that is valid in all cases. A common case that has been used in calculating typical chip power for the SA-110 is described next. Designers concerned about pin power in different cases are encouraged to use the expected switching characteristics of their design to calculate a value for pin power that is more appropriate to their application.

5.1.1 Cache Hit Rates

First, consider a program running on the SA-110 with an Icache hit rate of Hit_I and a Dcache hit rate of Hit_D. Twenty percent (20%) of the instructions are loads and 10% are stores, and the misses in the Dcache are divided between load and store misses in the ratio of 2 to 1.

The Dcache is fully loaded and half of the Dcache load misses are to blocks that are marked dirty so that half of the Dcache misses require a castout of a full block (8 words) before the fill can occur. The pin activity is assumed to be dominated by operations required to service these misses so that the bus accesses are all burst reads and writes of eight words each.

Consider the average activity on the bus over a period of time, which includes 100 non-fill CPU cycles. During this period, the SA-110 will do Nbw eight word burst writes, where Nbw is:

Nbw = 100 * [0.2 * (1-Hit_D)]

Additionally, in the same 100 non-fill CPU cycles, the SA-110 will do Nbr eight word burst reads, where Nbr is:

Nbr = 100 * {[0.2 * (1-Hit_D)]+(1-Hit_I)}

5.1.2 Number of Pin Transitions

Next, we need to make an assumption about the number of pin transitions associated with each burst read and write. Because address and data pins dominate the pin count, we only count these.

The SA-110 drives the address pins on reads and writes. For the first cycle of the burst, assume that half of the 32 address pins transition. For subsequent bus cycles, only the lowest 3 bits change and 11 pin transitions are required to step through the required addresses. This results in a total of 27 address pin transitions for an eight word burst read or write.

During writes, the SA-110 drives the data pins. Assuming half the data pins transition during each bus cycle of the access, 128 data pin transitions take place during each eight word burst write.

5.1.3 Memory Access Time

The final bit of information required to calculate the average pin power is the memory access time required for an eight word burst read or write. This can be expressed as a number of effective MCLK cycles so that it can be related to the bus speed. An effective MCLK cycle count should correspond to time, so that if the system uses nWAIT or stretches MCLK to provide additional time for a memory access, the number of effective MCLK cycles continues to increment. The number of MCLK cycles required for a burst read or write, Nburst, will depend on the design of the memory controller, the speed of the memory, and the MCLK frequency. The time period over which this activity occurs is:

Time interval (S) = 1e-6 * {[100/CPU freq (MHz)] + [Nburst * (Nbr + Nbw)/Bus freq (MHz)]}

The number of transitions is:

(Nbr * 27) + (Nbw * (128 + 27))

The pin power is:

$C * V^2 * f$

where:

C (F) = Total cap switched through a full cycle in this period
= 0.5 * [(Nbr * 27) + (Nbw * 155)] * C (F) on pins

V (v) = External **Vdd** (**Vddx**) = 3.3 V nominal

f (Hz) = 1/(Time interval in S)
= 1e-6/{[100/CPU freq (MHz)] + [Nburst * (Nbr + Nbw)/Bus freq (MHz)]}

The calculations just presented are for the data and address lines only.

Given the number of approximations that were made to generate these estimates, neglecting the control signals is probably acceptable. However, if the system in question drives MCLK (and possibly nMCLK) from the SA-110, the power associated with these pins should be included in the I/O power estimate. Because in normal mode these signals always toggle, the procedure for estimating the MCLK and nMCLK power is straightforward.

5.2 Typical Power Calculations

The power dissipated in the Dhrystone 2.1 loop is significantly higher than the power observed in most real applications. This is primarily because misses in the caches cause the internal CPU clock to switch to the bus clock during fills.

Given the calculations described in the previous section, it is possible to estimate an internal power that is closer to typical by including the effect of fills on the period over which the Dhrystone power is dissipated.

Note: The I/O power just calculated must be added to the following internal power calculated to obtain the total power consumption.

The typical internal power for a given hit rate and bus cycle time may be estimated by making the Dhrystone 2.1 power with no misses, scaling it up to account for the additional chip cycles associated with servicing the misses, and scaling the power down based on the time that it would take to execute this code with misses and the associated cache fills.

$$\text{Typical Internal Power} = \frac{\text{Dhrystone 2.1 power} * \{[100 + (8 * (\text{Nbr} + \text{Nbw}))]/100\} * [100/\text{CPU freq (MHz)}]}{\{[100/\text{CPU freq /(MHz)}] + [\text{Nburst} * (\text{Nbr} + \text{Nbw})/\text{Bus freq (MHz)}]\}}$$

5.3 dc Power Components

For applications that run at a low frequency, the ac operating power may be low enough that the two dc components of the SA-110 power become significant. These dc components are due to bias networks in the pad drivers and the leakage current of the transistors.

For the AA and BA parts, which are likely to be used in these low-power situations, the Idle power, which contains these two elements, is guaranteed to be no more than 20 mW. The power due to these dc sources is included in the power estimates previously described, but it is insignificant compared to the ac power unless the frequency is very low. This dc power should be considered if the calculations above result in a power comparable to 20 mW.

5.4 dc Pin Current

These estimates do not include an allowance for power associated with sinking or sourcing dc current from the output drivers. There is also an assumption that inputs to the SA-110 are driven to the external power rails so that no appreciable power in the input receivers exists.

6 Support, Products, and Documentation

If you need technical support, a *Digital Semiconductor Product Catalog,* or help deciding which documentation best meets your needs, visit the Digital Semiconductor World Wide Web Internet site:

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You can also call the Digital Semiconductor Information Line or the Digital Semiconductor Customer Technology Center. Please use the following information lines for support.

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For technical support:	
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Fax:	1–508–568–6698
Electronic mail address:	ctc@hlo.mts.dec.com

Digital Semiconductor Products

To order the Digital Semiconductor SA-110 microprocessor, contact your local distributor.

Product	Order Number
Digital Semiconductor SA-110 100 MHz Microprocessor	21281–BA
Digital Semiconductor SA-110 160 MHz Microprocessor	21281–AA
Digital Semiconductor SA-110 166 MHz Microprocessor	21281–DA
Digital Semiconductor SA-110 200 MHz Microprocessor	21281–CA
Digital Semiconductor SA-110 233 MHz Microprocessor	21281–EA

Digital Semiconductor Documentation

The following table lists some of the available Digital Semiconductor documentation. For a complete list, call the Digital Semiconductor Information Line.

Title	Order Number
Digital Semiconductor SA-110 Microprocessor Tools Brochure	EC–QPWJB–TE
Digital Semiconductor SA-110 Microprocessor for Embedded Applications Product Brief	EC–QPWKD–TE
Digital Semiconductor SA-110 Microprocessor for Portable Applications Product Brief	EC–R2WWA–TE
Digital Semiconductor SA-110 Microprocessor Technical Reference Manual	EC–QPWLC–TE
Digital Semiconductor SA-110 Microprocessor Evaluation Board Reference Manual	EC–QU5KA–TE
Digital Semiconductor EBSA-110 Hardware Developer's Kit Read Me First	EC–QU9ZA–TE
ARM Architecture Reference Manual	EC–QV44A–TE

Title	Order Number
StrongARM Internet Appliance Evaluation Board Programming Manual	EC–R2NJA–TE
StrongARM Internet Appliance Evaluation Board Theory of Operation	EC–R2NKA–TE
Memory Management on the StrongARM SA-110: An Application Note	EC–R4WCA–TE