BAN#=EBSA-110 - STRONGARM EVALUATION BOARD
REV#=REVB

EBSA-110 Schematic Directory

SHEET	SIG PREFIXES	DESCRIPTION
sht 1	-	Schematic Directory
sht 2	-	Block diagram
sht 3	CPU_, ECH_, 3V3_	CPU, clock, level-shifting
sht 4	-	Debug pick-up points
sht 5	-	SSRAM
sht 6	BUF_, IO_	Address and data buffering
sht 7	MUX_, SIM_	DRAM address MUXing and SIMMs
sht 8	CTA_, CTB_	Control state machines
sht 9	CTA_, CTB_	Series terminations and decoupling for sht8
sht 10	ROM_	EPROM/Flash with byte->word packer
sht 11	SUP_, CON_	Super I/O
sht 12	MAX_, IND_, CON_	Super I/O RS232 drivers and connectors
sht 13	NET_	Ethernet controller with clock & LEDs
sht 14	-	Ethernet buffer RAM and address ROM
sht 15	-	Ethernet media interface
sht 16	CIA_	PCMCIA controller
sht 17	PWA_, PWB_, SLA_, SLB_	PCMCIA connector and power control
sht 18	TAG_, RST_, BUF_	JTAG connector & buffers, reset circuitry
sht 19	PIT_, SPR_	Timer (PIT), spare gates, CPU decoupling
sht 20	-	Power regulation
sht 21	-	Power connectors and bulk decoupling
sht 22	LNK_, ANA_	Configuration jumpers

Note:
CTB_DBG (SHT 8)
has no fanout

JUMPERS

SHT20, SHT22

PICKUPS

SHT4, SHT20

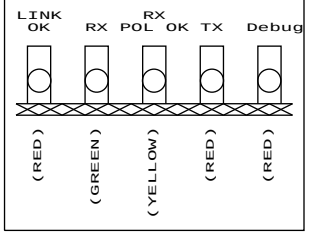
CONNECTORS

SHT12, SHT15, SHT17
SHT18, SHT21

LINKS

SHT3, SHT5, SHT19

LEDs



- All signals have a 3-letter prefix of their origin (for bidirects this is the arbitrarily Most Important Driver)
- Side-2 Etchlinks start at EL101
- Side-2 capacitors start at C301
- All other components are on side 1

2-13-1996_18:33

REVISION		
CHK	CHANGE NO.	REV

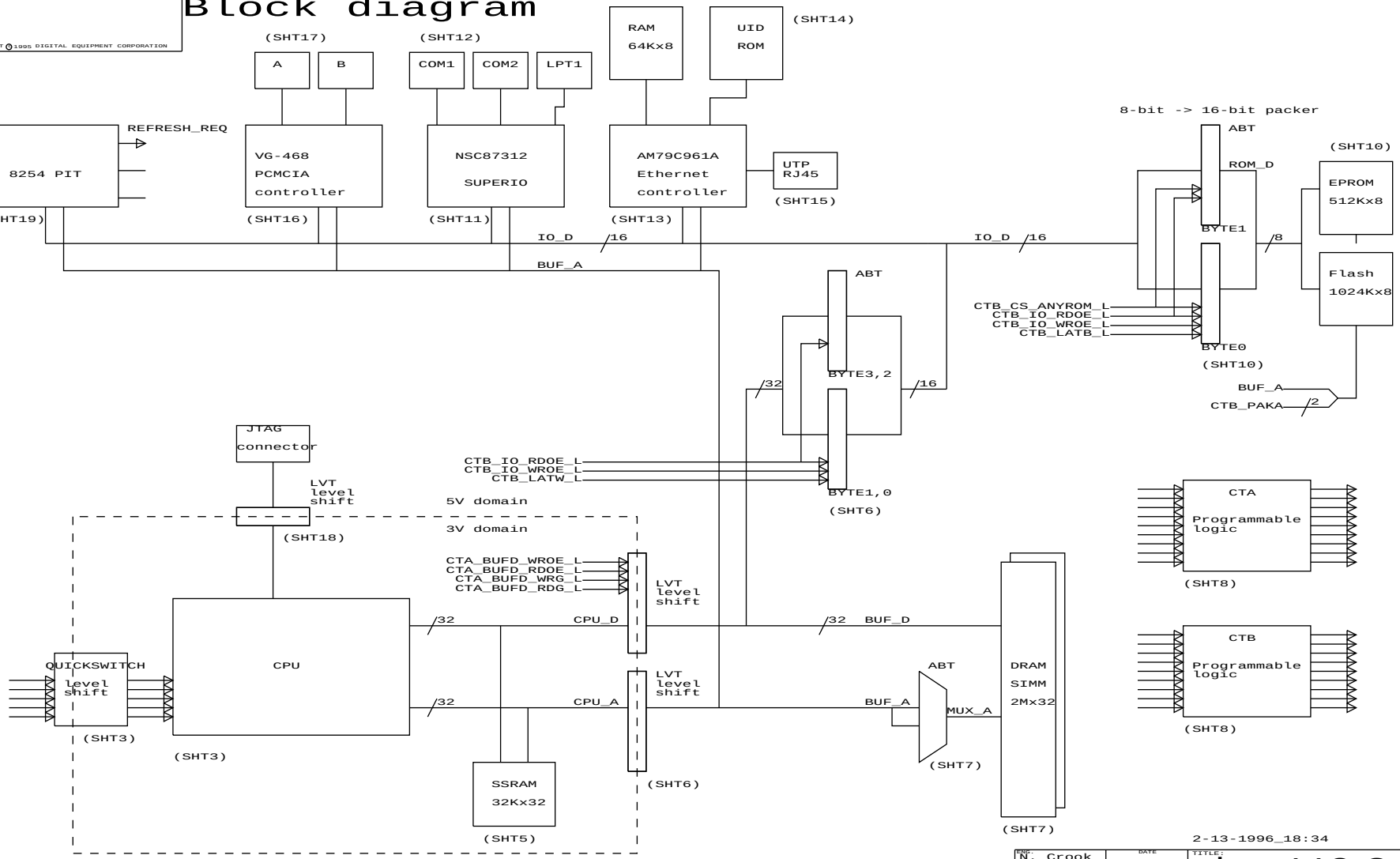
digital

DRN. DATE
CHK'D. DATE
USRA:
FIRST USED ON OPTION/MODEL:

ENG. N. Crook DATE
BOARD LOCATION:
SHEET 1 OF
TOP DOCUMENT NUMBER:

TITLE: ebsa110 1
SIZE B | CODE | NUMBER | REV.

Block diagram



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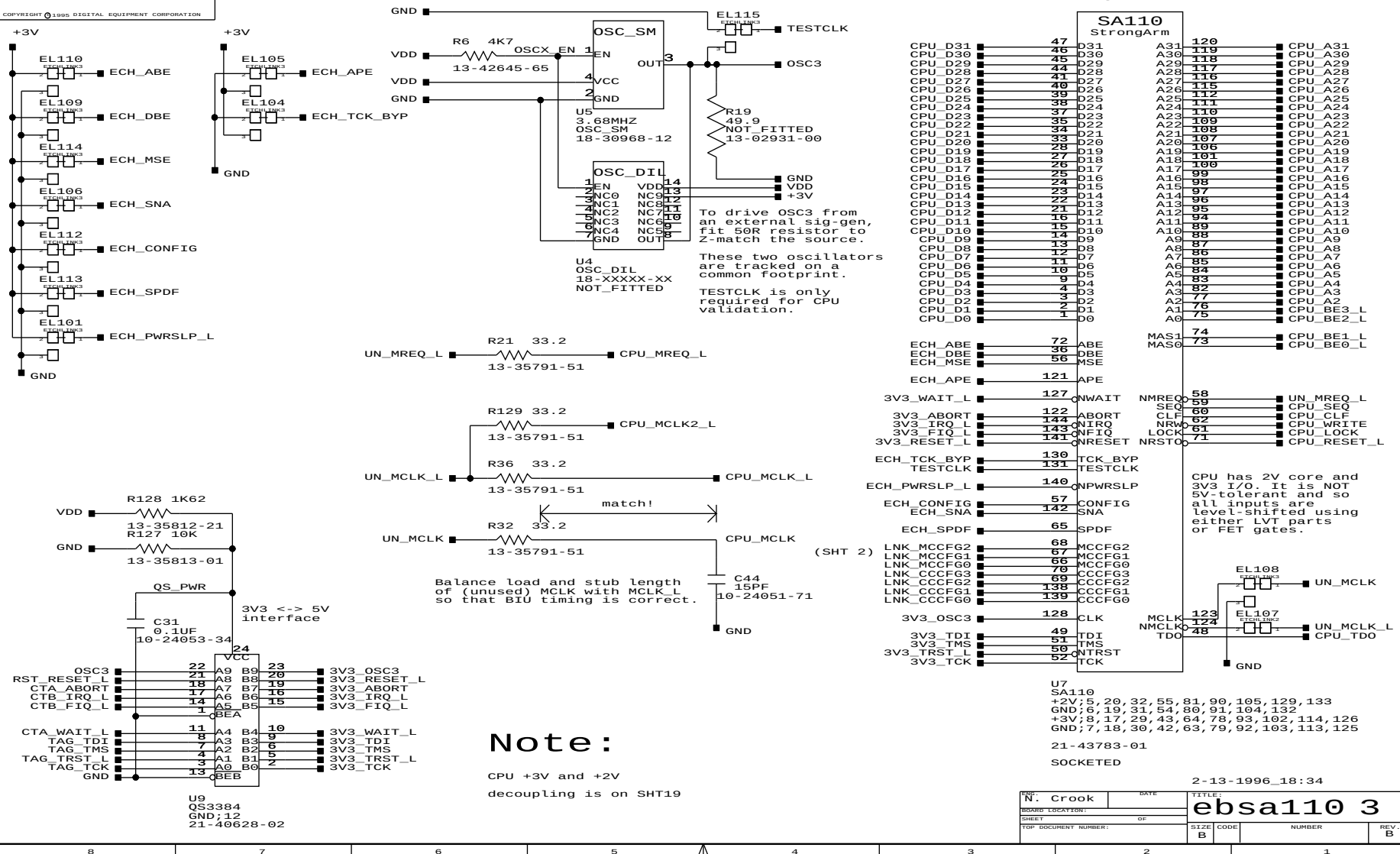
ENG: N. Crook	DATE	TITLE: ebsa110 2	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

CPU, clock, level shift & decouplers



Note:

CPU +3V and +2V

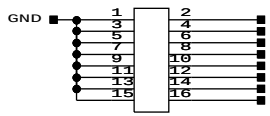
decoupling is on SHT19

2-13-1996_18:34

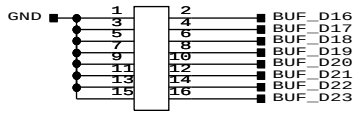
ENG: N. Crook	DATE	TITLE: ebsa110 3	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

CPU pickups

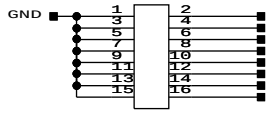
These connectors are pinned to directly connect to a Tektronix DAS logic analyser



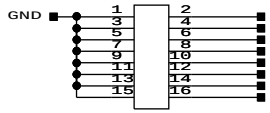
J7
HEAD8X2
12-13488-13



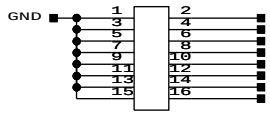
J9
HEAD8X2
12-13488-13



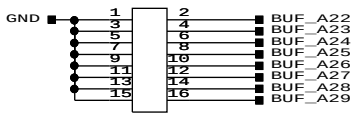
J8
HEAD8X2
12-13488-13



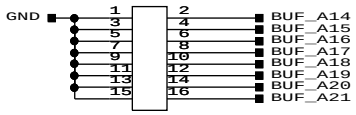
J10
HEAD8X2
12-13488-13



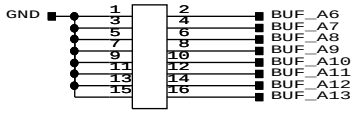
J11
HEAD8X2
12-13488-13



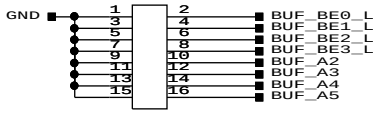
J18
HEAD8X2
12-13488-13



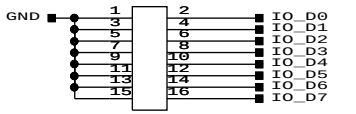
J14
HEAD8X2
12-13488-13



J15
HEAD8X2
12-13488-13

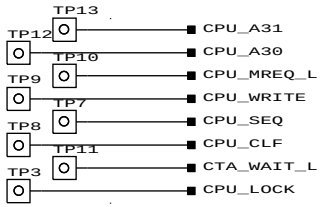


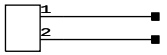
J16
HEAD8X2
12-13488-13



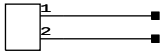
J12
HEAD8X2
12-13488-13

These test points are intended to be big VIAs on the normal daisy-chained etch in order to provide pickup without adding etch length or capacitive load

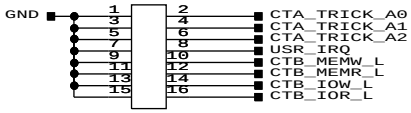




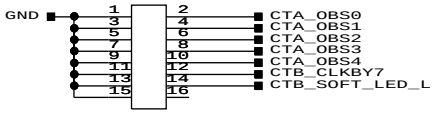
J27
12-15901-05
NOT_FITTED



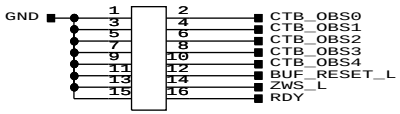
J28
12-15901-05
NOT_FITTED



J19
HEAD8X2
12-13488-13

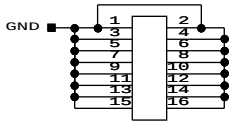


J17
HEAD8X2
12-13488-13

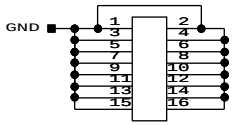


J13
HEAD8X2
12-13488-13

OV pickups for DAS



J29
HEAD8X2
12-13488-13
NOT_FITTED



J26
HEAD8X2
12-13488-13
NOT_FITTED

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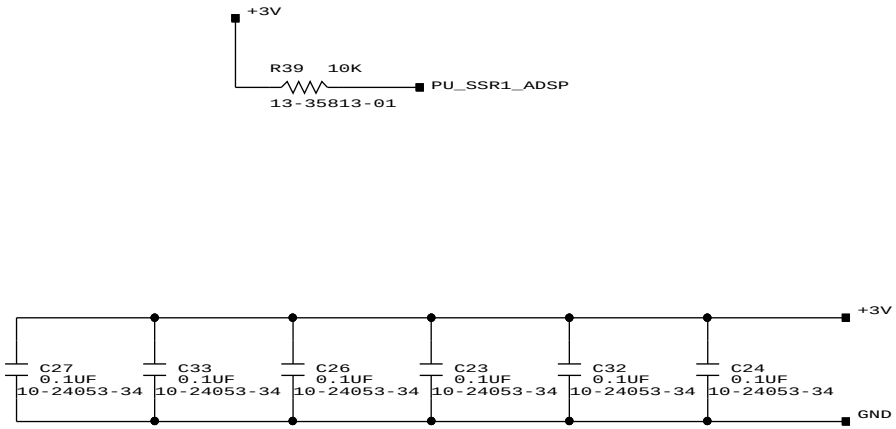
ENG. N. Crook	DATE	TITLE: ebsa110 4
BOARD LOCATION:		
SHEET OF		
TOP DOCUMENT NUMBER:		SIZE B / CODE / NUMBER / REV. B

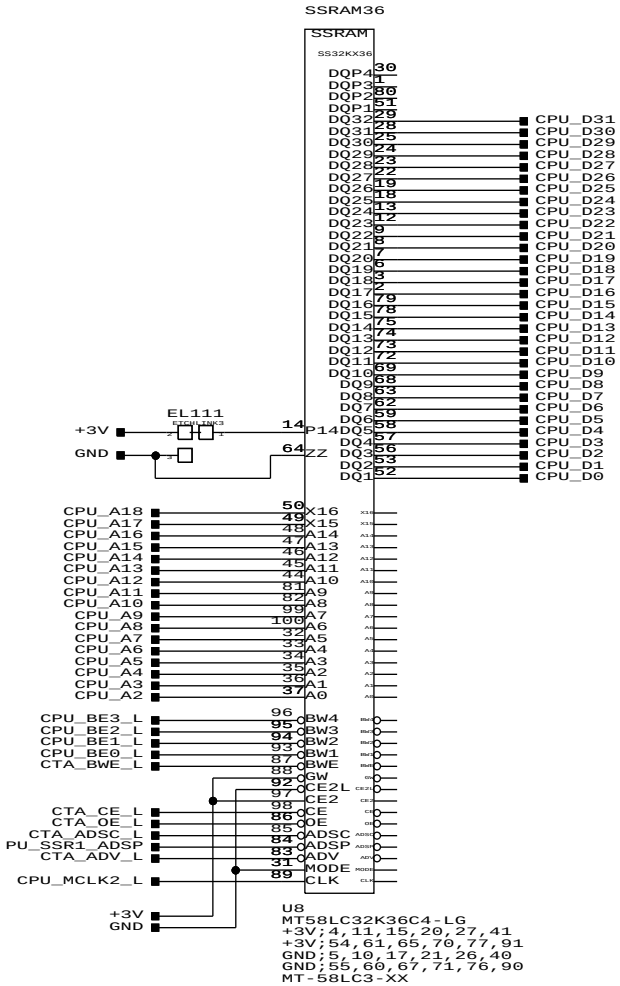
SSRAM

This synchronous SRAM
has registered outputs

Fit either 32Kx32 or 32Kx36 part

The wiring of pins 14, 64 is
intended to accommodate the
next-generation parts,
64Kx36. A micron MT58LC64K36C4
or MT58LC64K36D7 should be OK.





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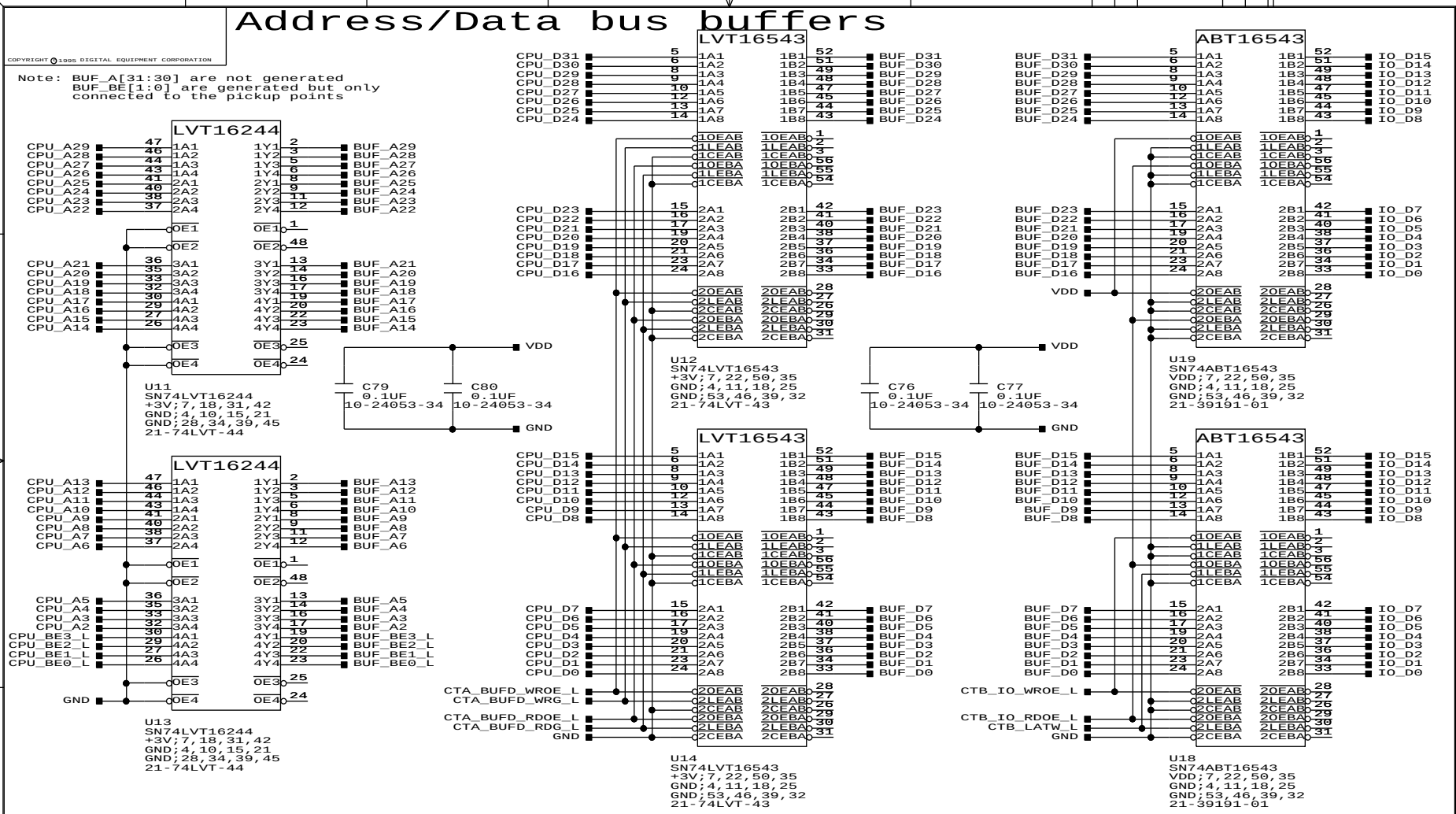
ENG. N. Crook	DATE	TITLE: ebsa110 5	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

Address/Data bus buffers

Note: BUF_A[31:30] are not generated
BUF_BE[1:0] are generated but only
connected to the pickup points

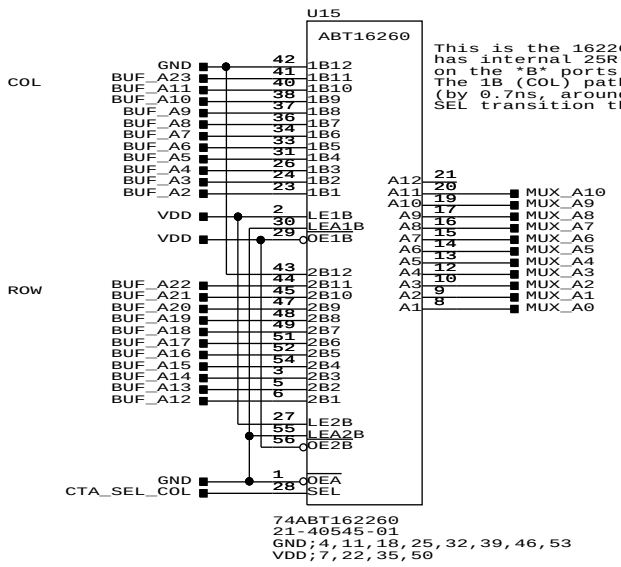


2-13-1996_18:35

ENG: N. Crook	DATE	TITLE: ebsa110 6	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B

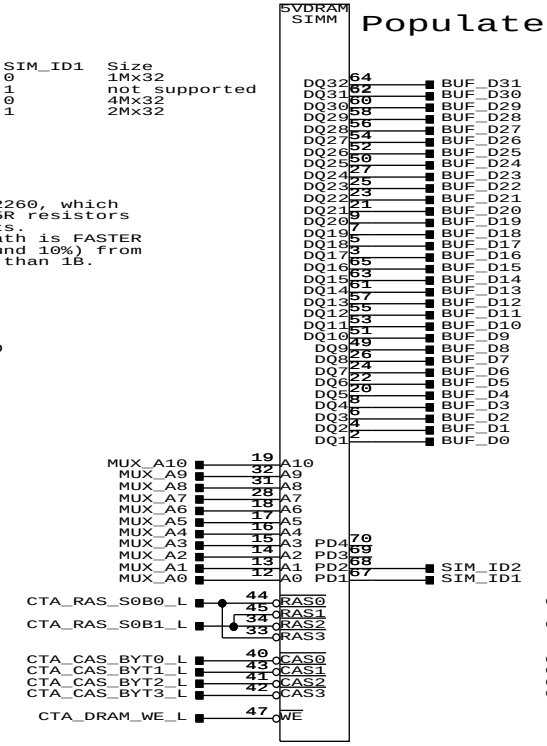
DRAM SIMMS & address MUX

SIM_ID2	SIM_ID1	Size
0	0	1Mx32
0	1	not supported
1	0	4Mx32
1	1	2Mx32



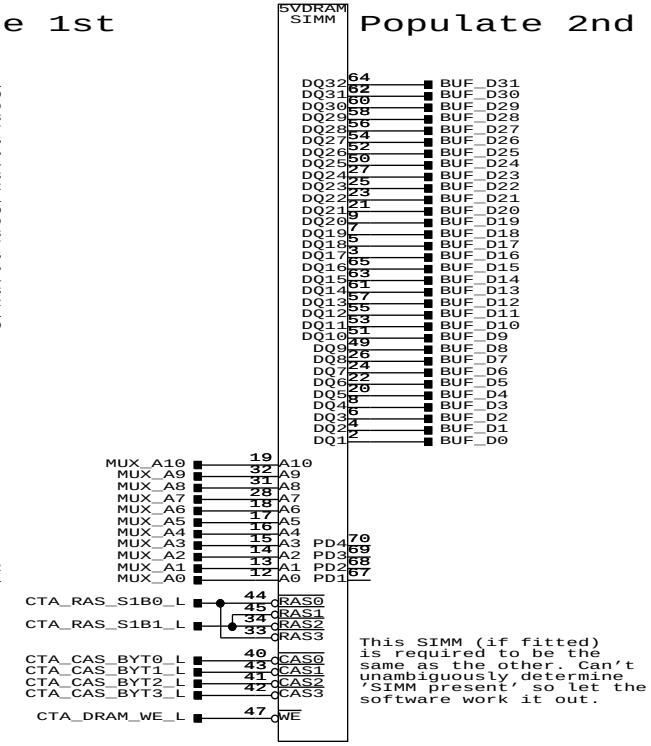
This is the 162260, which has internal 25R resistors on the *B* ports. The 1B (COL) path is FASTER (by 0.7ns, around 10%) from SEL transition than 1B.

74ABT162260
21-40545-01
GND;4,11,18,25,32,39,46,53
VDD;7,22,35,50



J6
DSIMM32
12-34138-06

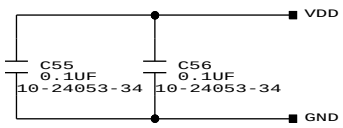
VDD;10,30,59
GND;1,39,72

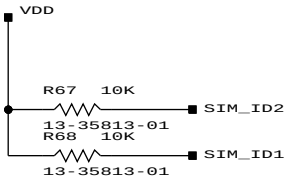


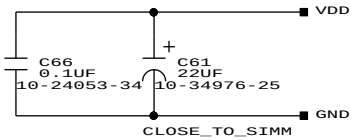
This SIMM (if fitted) is required to be the same as the other. Can't unambiguously determine 'SIMM present' so let the software work it out.

J5
DSIMM32
12-34138-06

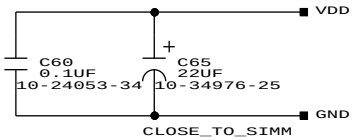
VDD;10,30,59
GND;1,39,72







This is the DPN for the 72-pin socket.



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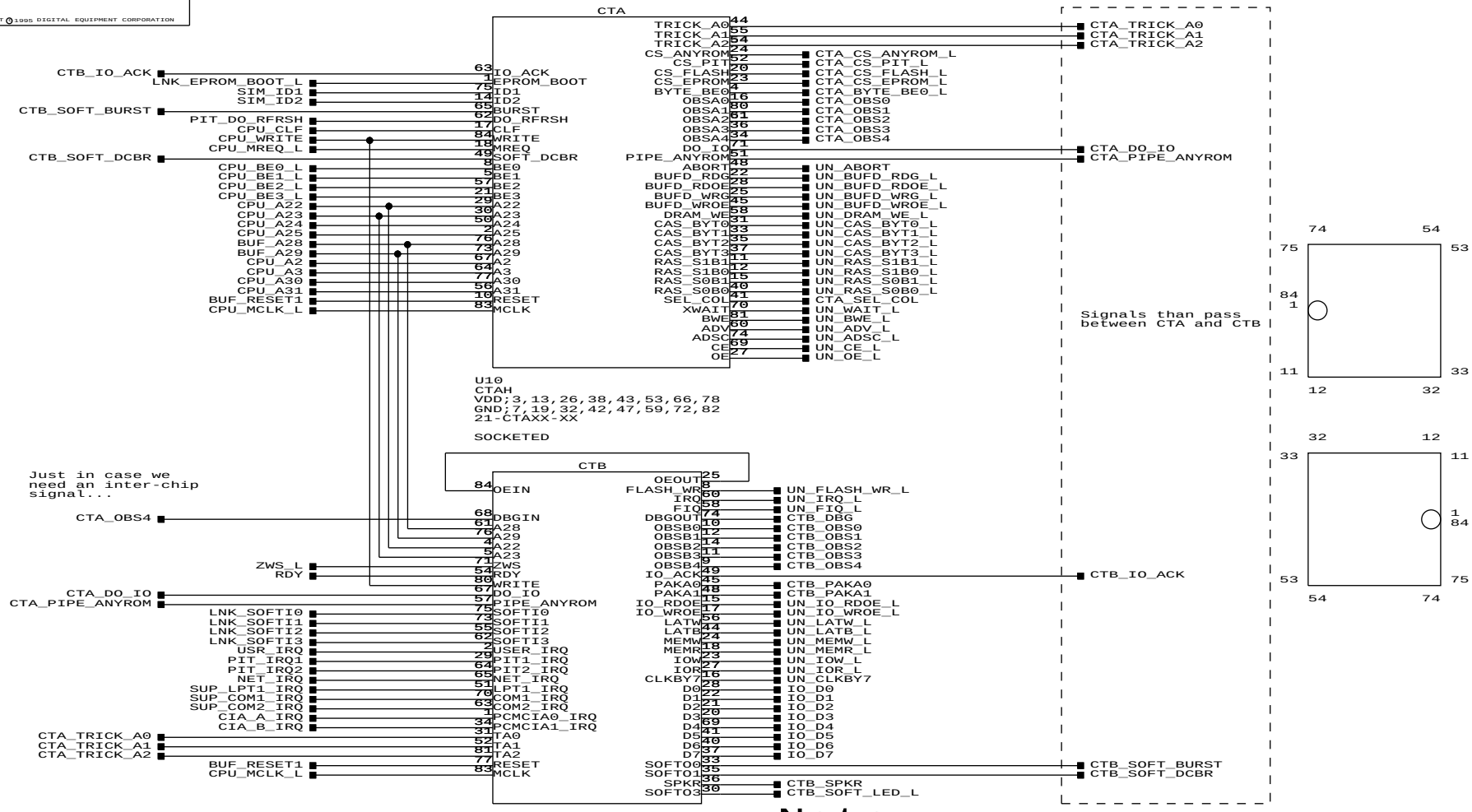
ENG: N. Crook	DATE	TITLE: ebsa110 7	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B / CODE / NUMBER	REV. B

Control logic for SSRAM, DRAM, RFRSH, I/O.



Notes:

Both parts are Altara EPM7096LC84-7.

Signals prefixed UN_ have series terminations on SHT9.

Decoupling is on SHT9.

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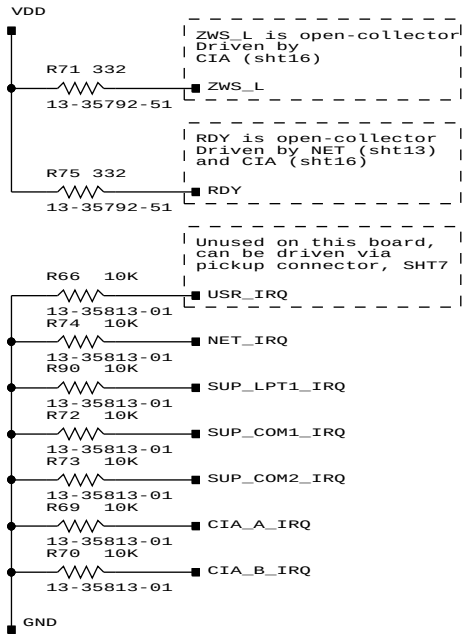
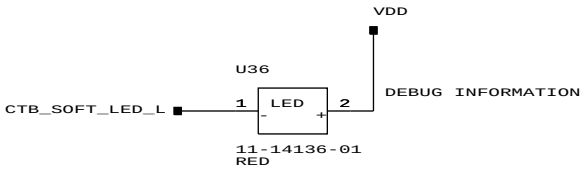
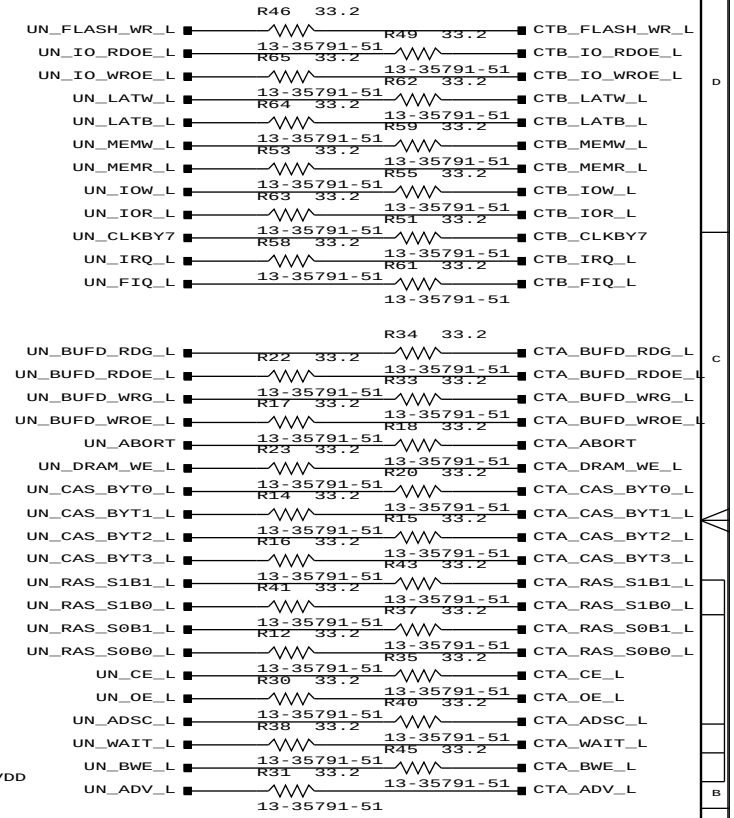
ENG.	DATE	TITLE: ebsa110 8	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B

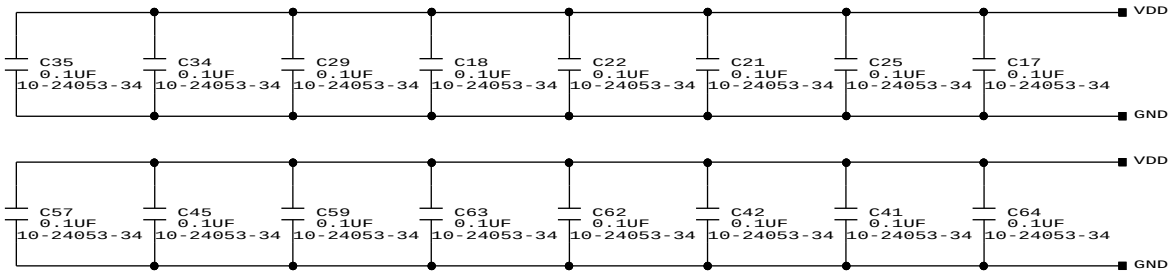
Control logic: terminations and decoupling







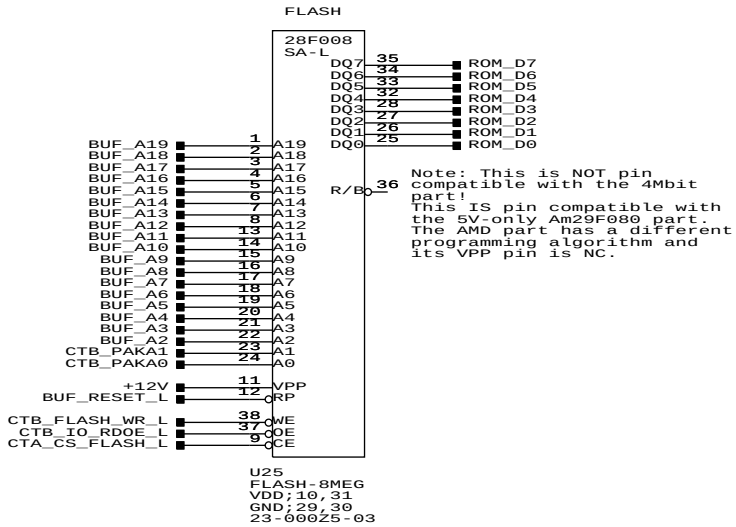
Decoupling for CTA, CTB on SHT8



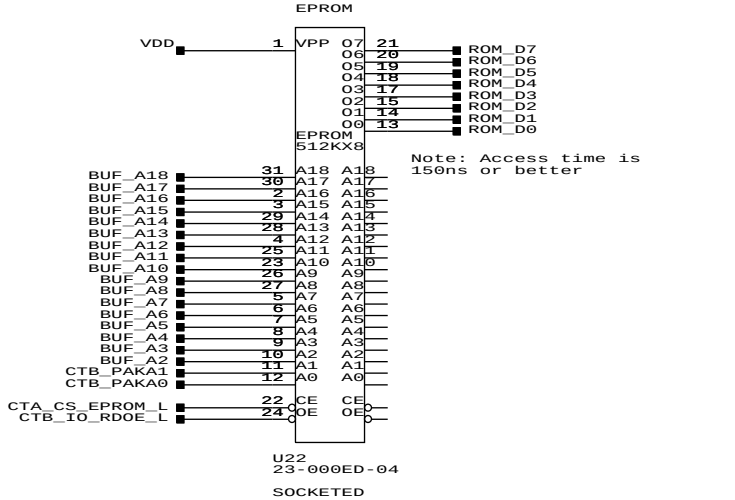
2-23-1996_11:13

ENG. N. Crook	DATE	TITLE: ebsa110 9	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B

EPROM packer



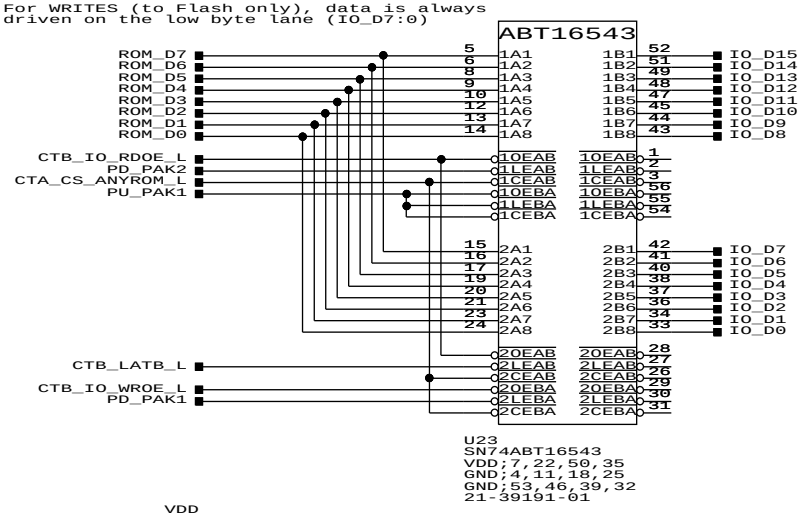
Note: This is NOT pin compatible with the 4Mbit part!
This IS pin compatible with the 5V-only Am29F080 part.
The AMD part has a different programming algorithm and its VPP pin is NC.

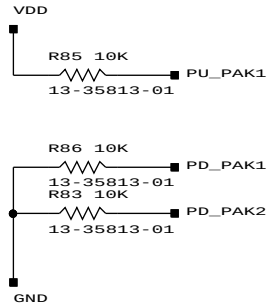


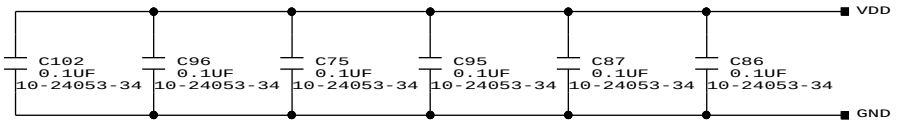
Note: Access time is 150ns or better

For READS, even-address bytes are latched into IO_D7:0 using LATB. This produces 16-bit values on IO_D which are packed into 32-bit values by the latches on sht6.

For WRITES (to Flash only), data is always driven on the low byte lane (IO_D7:0)







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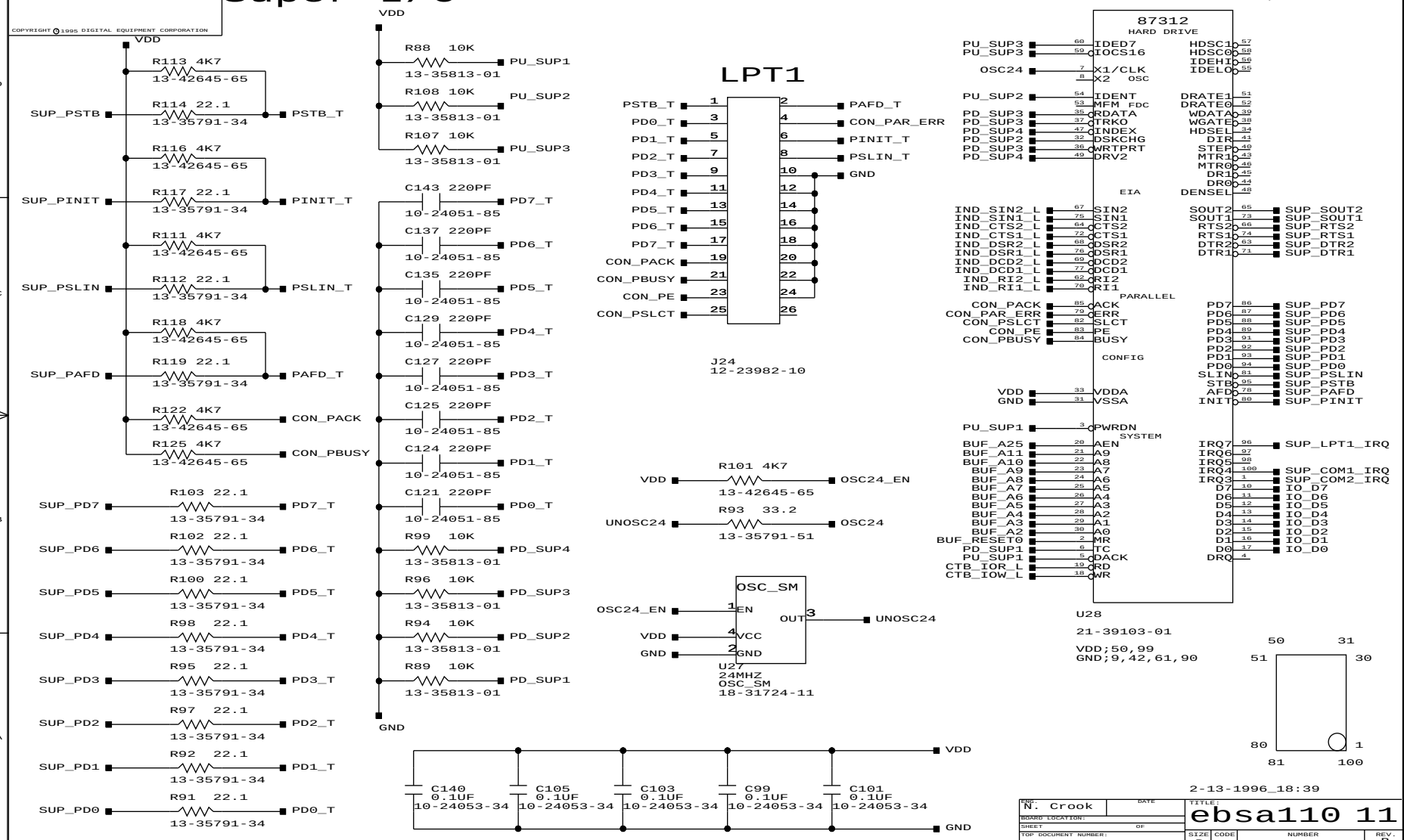
ENG. N. Crook	DATE	TITLE: ebsa110 10	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B

Super I/O

National PC87312 Combo chip



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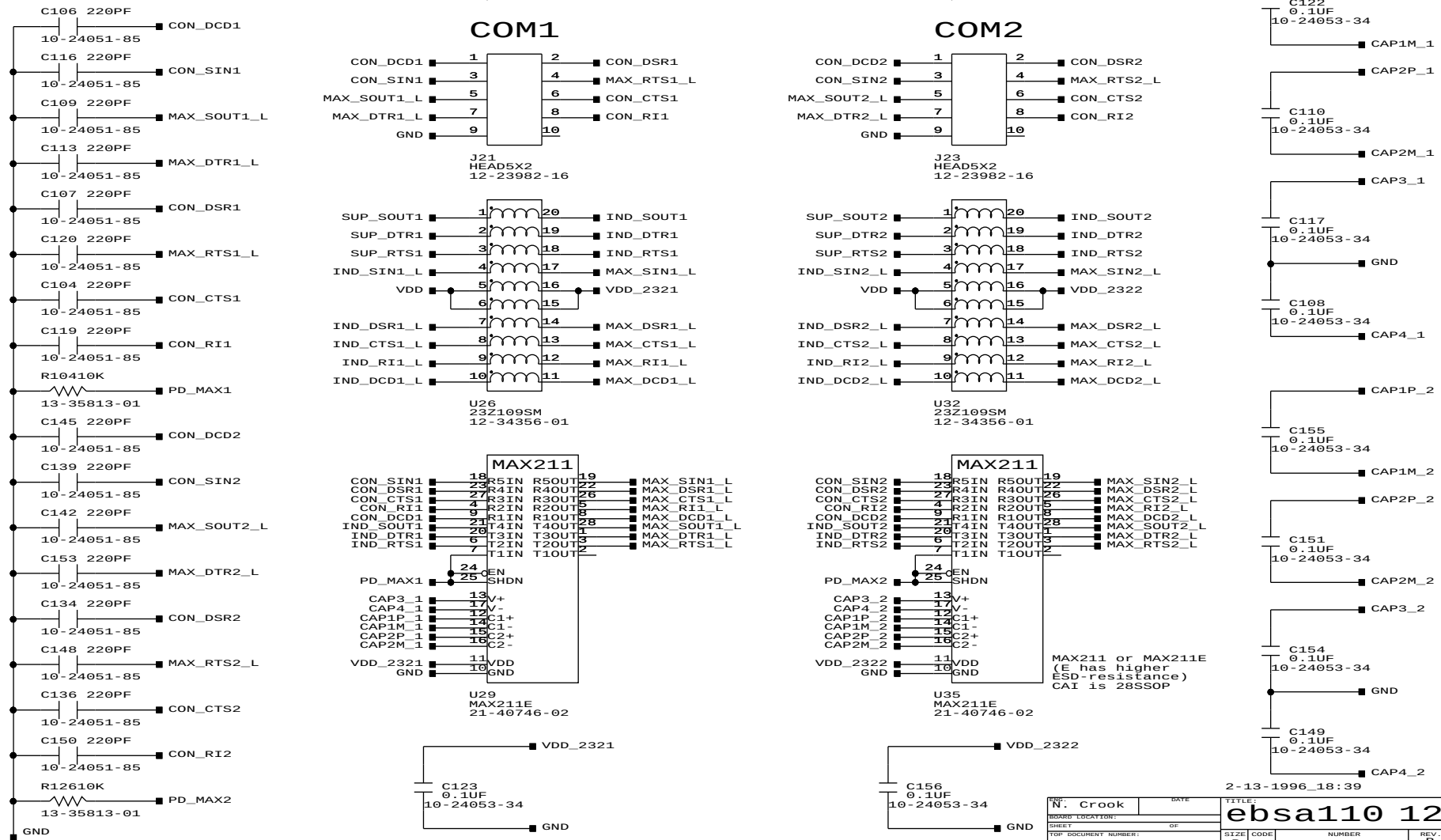
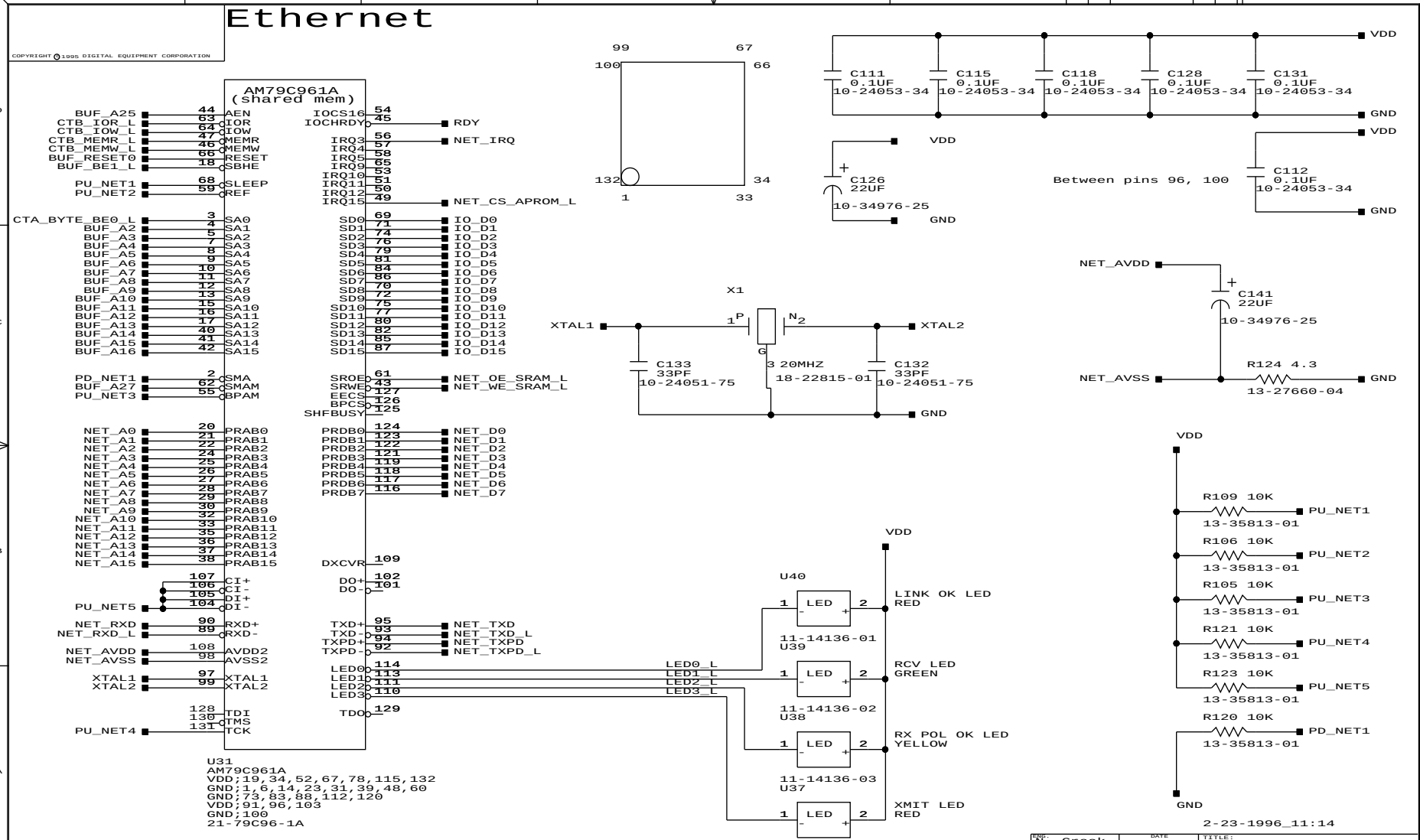
ENG: N. Crook	DATE	TITLE: ebsa110 11	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

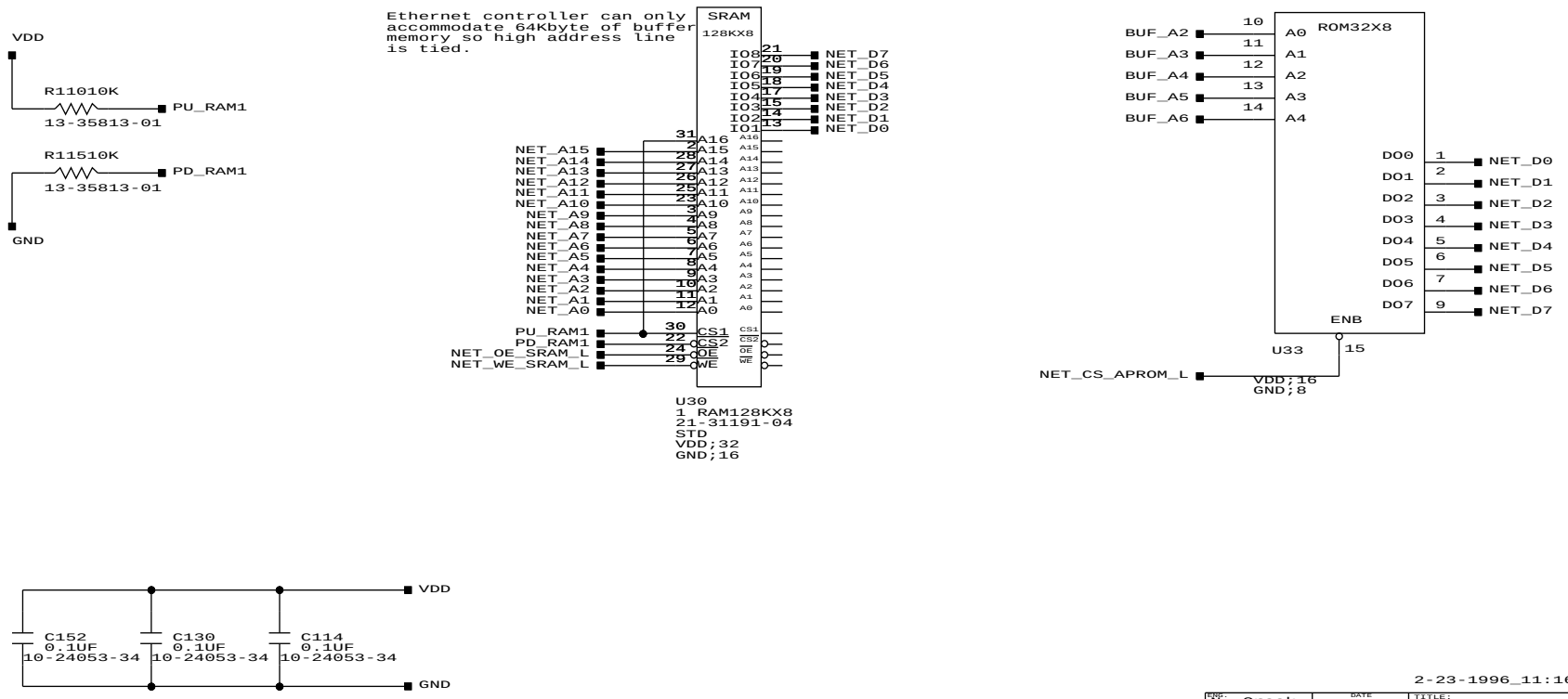
RS232 drivers and connectors



Ethernet



Ethernet buffer RAM and ID ROM



2-23-1996_11:16

ENG. N. Crook	DATE	TITLE: ebsa110 14	
BOARD LOCATION:			
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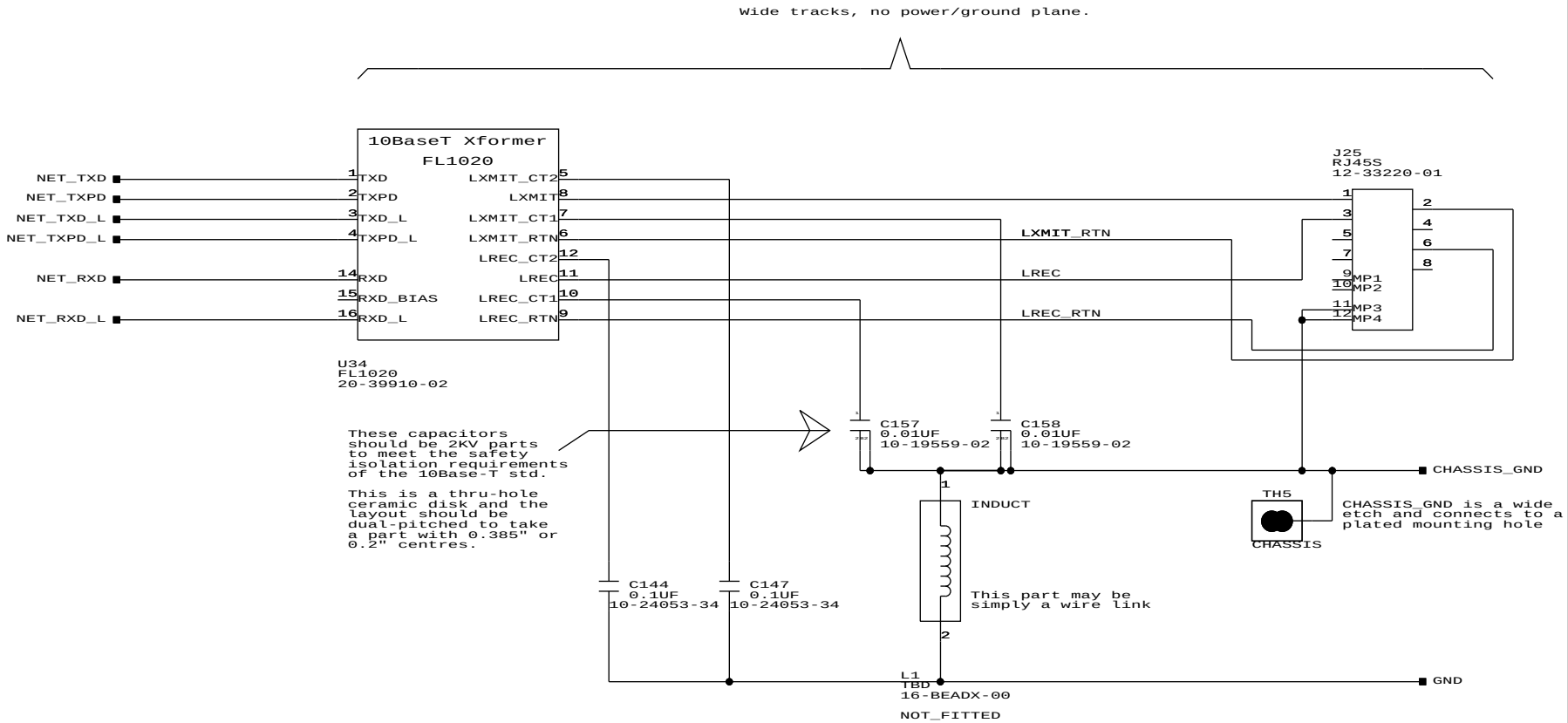
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

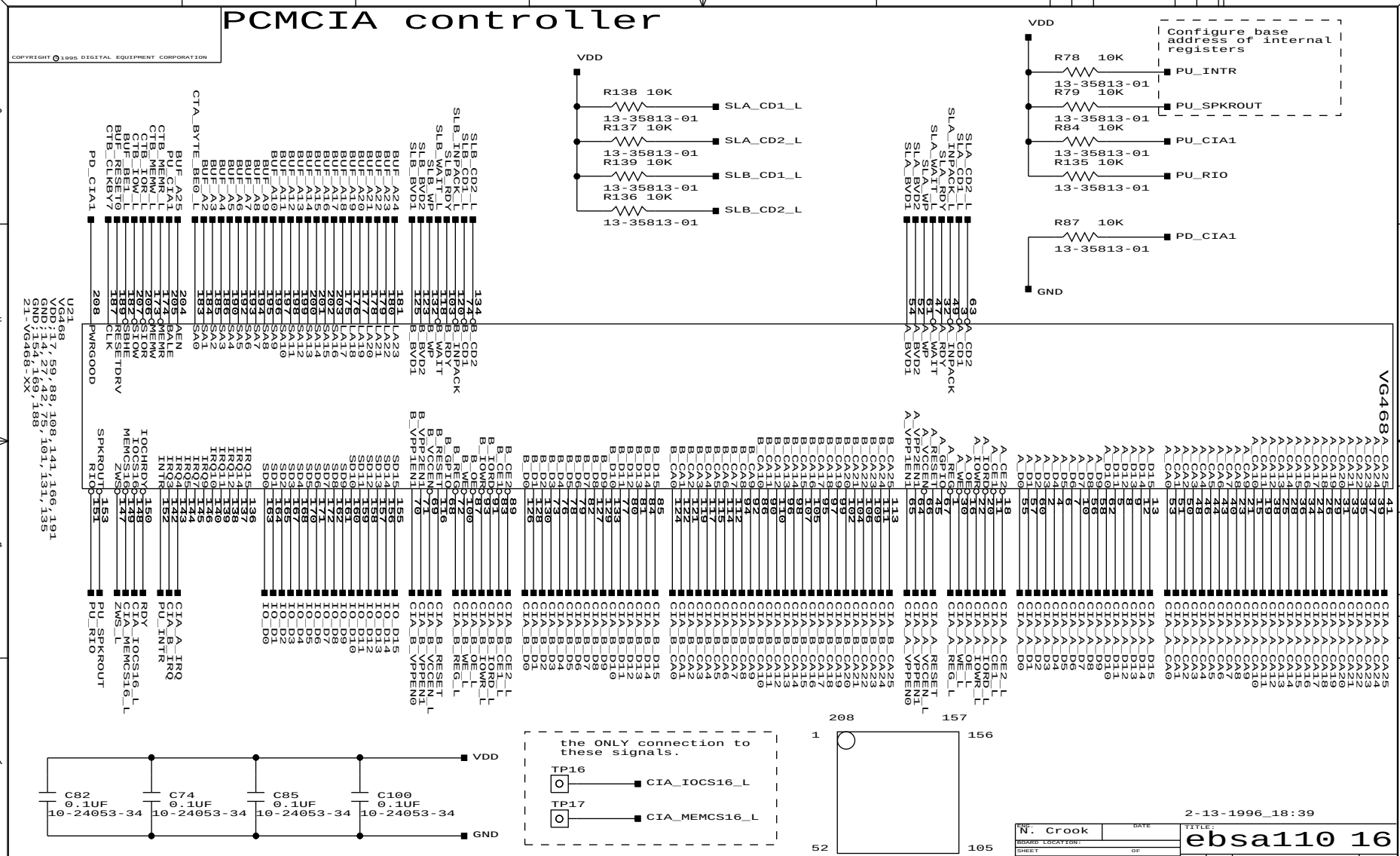
Ethernet - BalUn and media connection



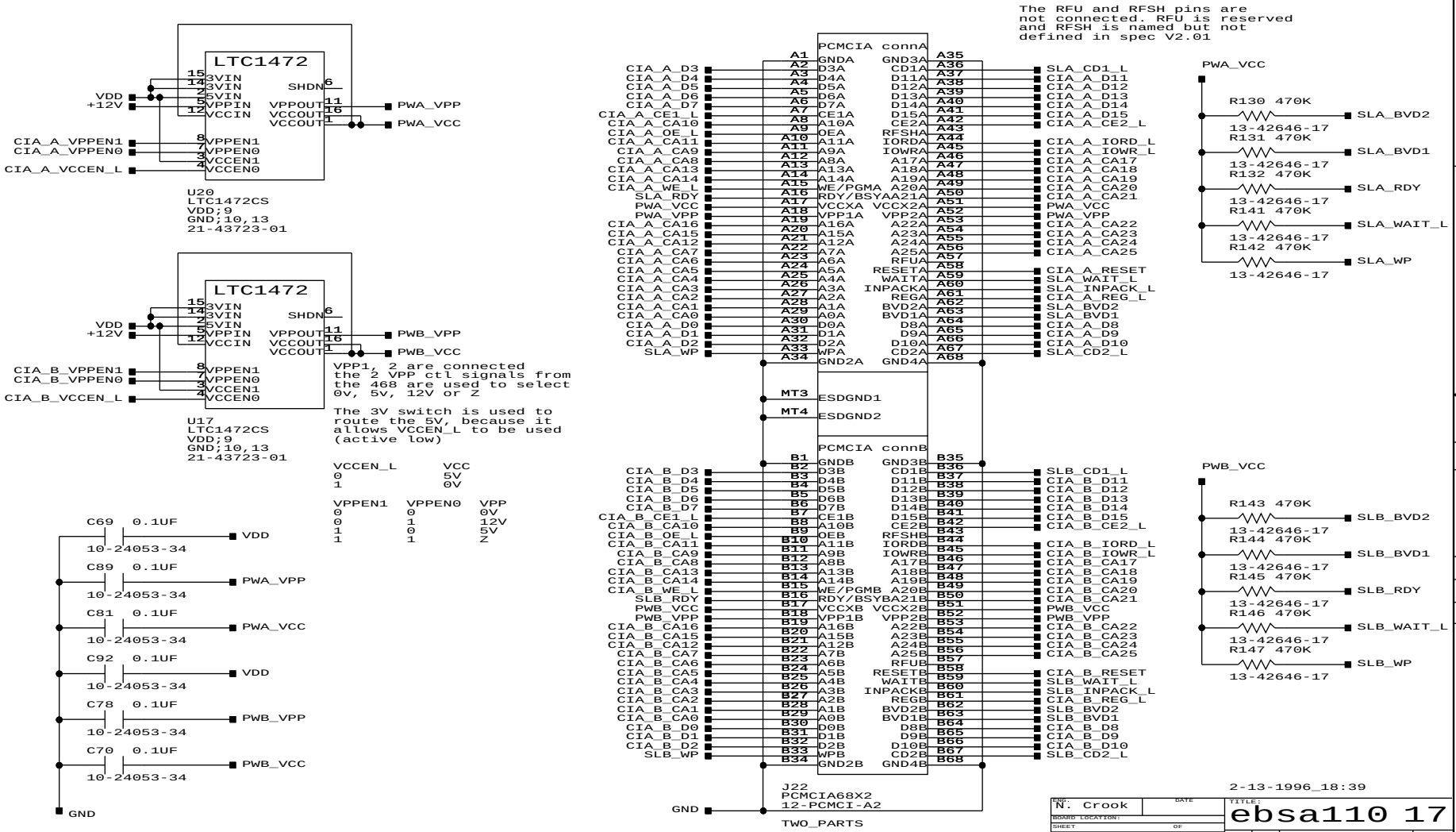
2-13-1996_18:39

ENG. N. Crook	DATE	TITLE: ebsa110 15	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B / CODE / NUMBER	REV. B

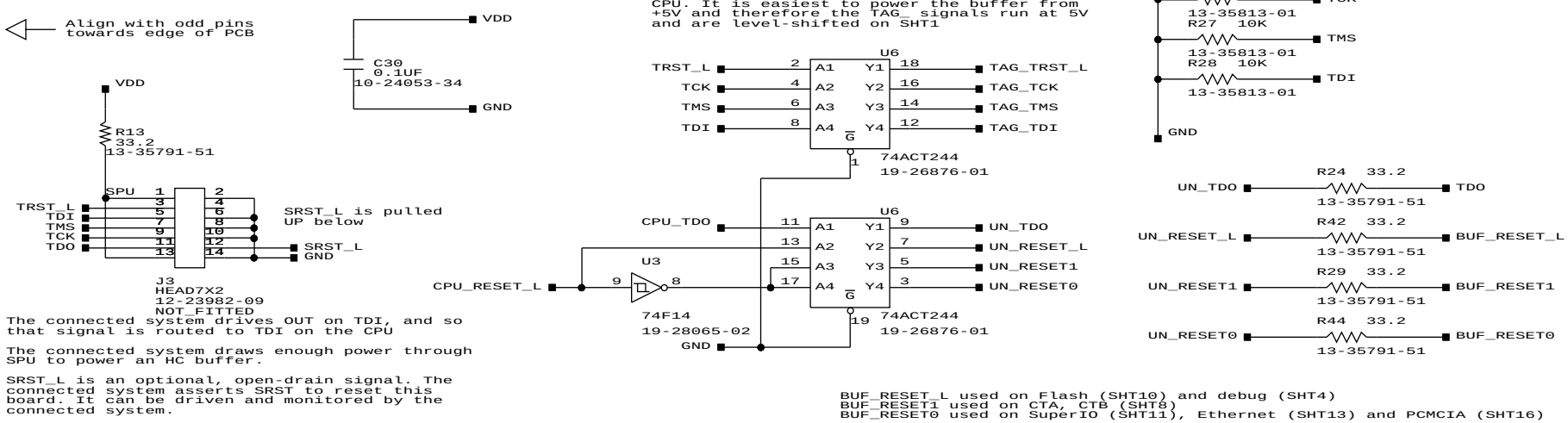
PCMCIA controller



PCMCIA connectors and power control



JTAG port (to CPU only)



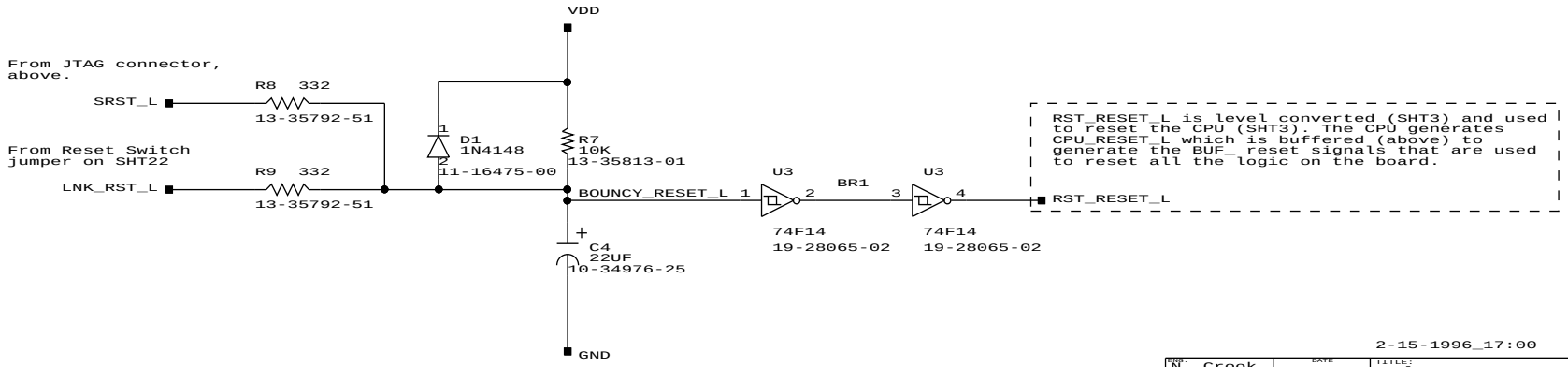
The connected system drives OUT on TDI, and so that signal is routed to TDI on the CPU

The connected system draws enough power through SPU to power an HC buffer.

SRST_L is an optional, open-drain signal. The connected system asserts SRST to reset this board. It can be driven and monitored by the connected system.

BUF_RESET_L used on Flash (SHT10) and debug (SHT4)
BUF_RESET1 used on CTA, CTB (SHT8)
BUF_RESET0 used on SuperIO (SHT11), Ethernet (SHT13) and PCMCIA (SHT16)

Reset



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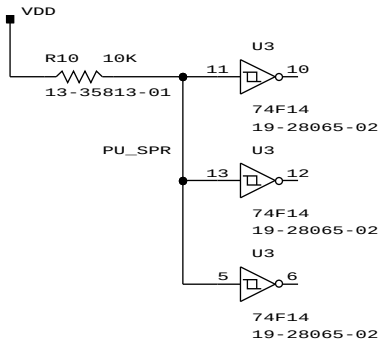
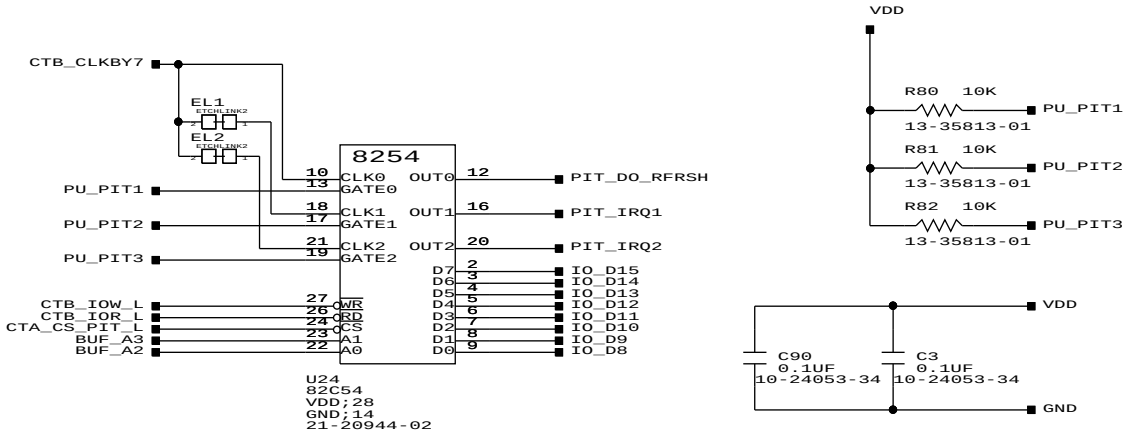
ENG: N. Crook	DATE	TITLE: ebsa110 18	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

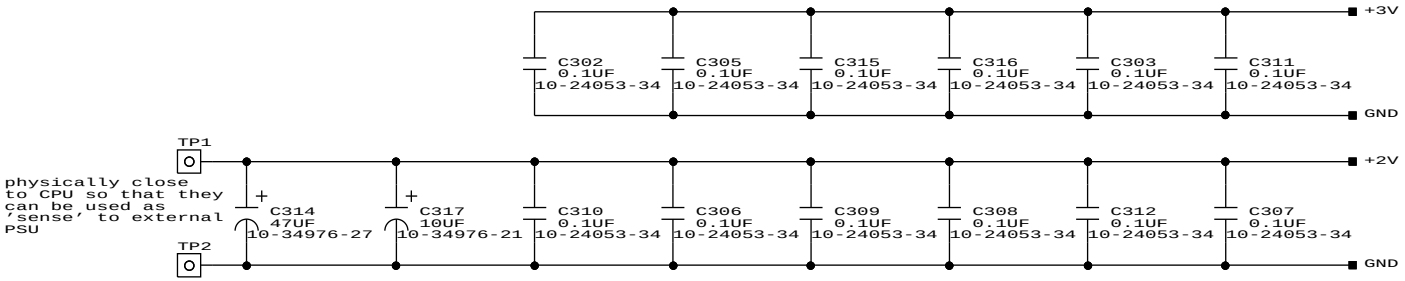
Spares



Counter/timer



Decoupling for CPU (sht 3)



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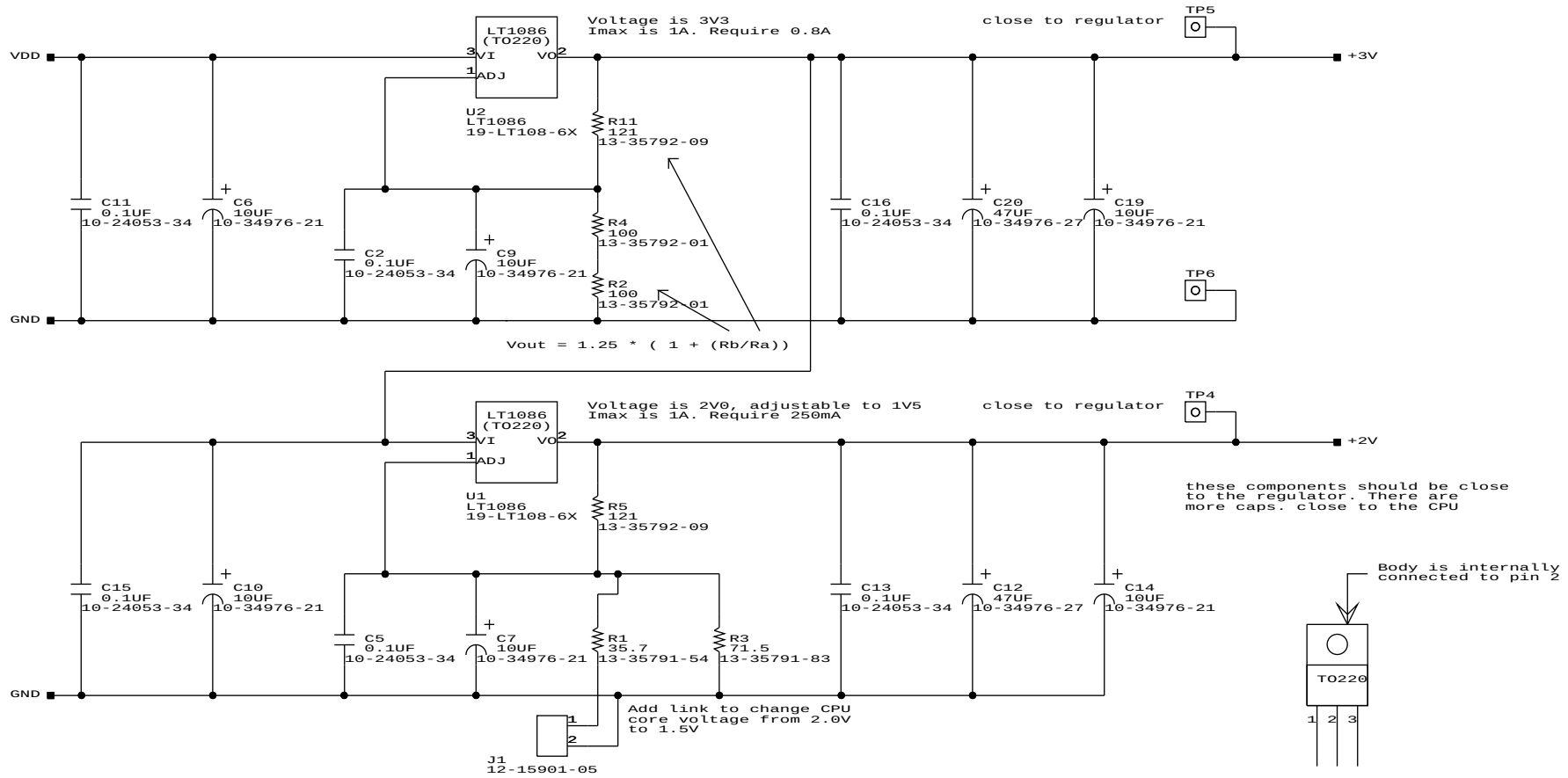
ENG. N. Crook	DATE	TITLE: ebsa110 19	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

Power regulation (3V3, 1.5V/2V)



heatsinks**

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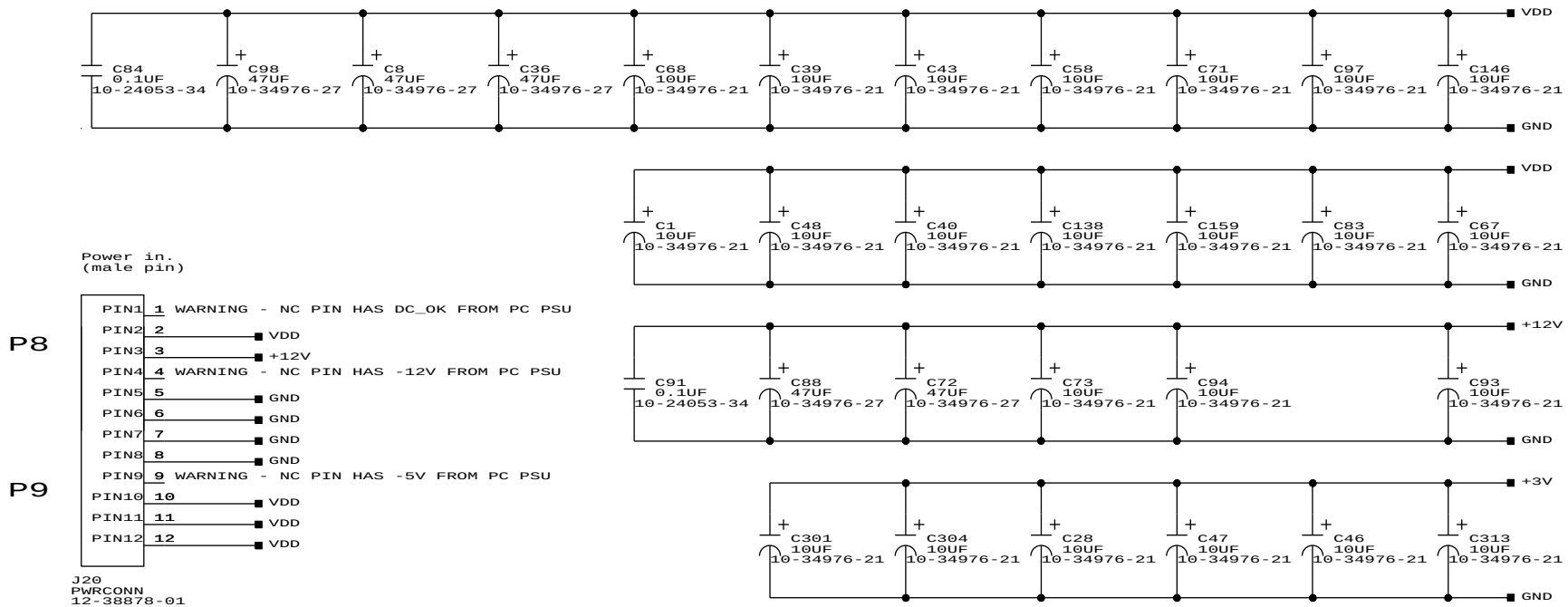
ENG. N. Crook	DATE	TITLE: ebsa110 20	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B

Decoupling; bulk, for all power planes



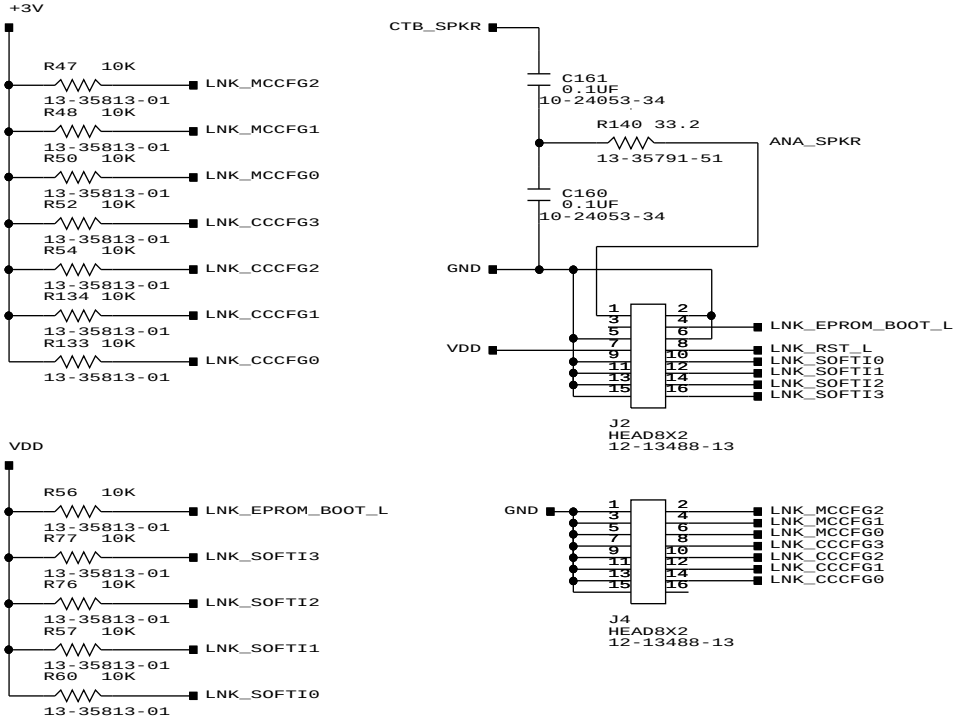
Power in.
(male pin)

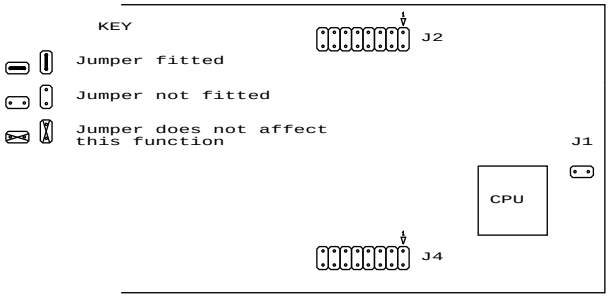
Note: +12V is 'optional'. The board will function with +5V only. +12V is required for programming the FLASH and may be required by a plug-in PCMCIA card.

2-13-1996_18:39

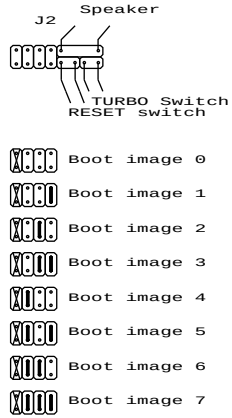
ENG. N. Crook	DATE	TITLE: ebsa110 21	
BOARD LOCATION:			
SHEET	OF		
TOP DOCUMENT NUMBER:		SIZE B	CODE	NUMBER	REV. B

Configuration Jumpers (See also SHT20)





J1	J4	Vcore	Fcore	Fbus
		+1.5V	88.3MHz	44.1MHz
		+1.5V	95.6MHz	47.8MHz
		+1.5V	99.4MHz	49.7MHz
		+1.5V	106.7MHz	53.3MHz
		+1.5V	143.5MHz	47.8MHz
		+1.5V	150.9MHz	50.3MHz
		+1.5V	161.9MHz	53.9MHz
		+1.5V	169.3MHz	42.3MHz
		+2.0V	191.3MHz	47.8MHz
		+2.0V	202.4MHz	50.6MHz
		+2.0V	213.4MHz	53.3MHz
		+2.0V	228.1MHz	45.6MHz
		+2.0V	242.8MHz	48.5MHz
		+2.0V	257.6MHz	51.5MHz
		+2.0V	276.0MHz	46.0MHz
		+2.0V	287.0MHz	47.8MHz



TURBO Switch - boot from FLASH when OFF from EPROM when ON.

3-1-1996_10:38

ENG. N. Crook	DATE	TITLE: ebsa110 22	
BOARD LOCATION:			
SHEET OF			
TOP DOCUMENT NUMBER:		SIZE B	CODE / NUMBER / REV. B